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Compiling Your Design

... vhd" analyze -format **vhdl** MOD10 + ".vhd" analyze -format **vhdl** TOP + ".vhd" ...
Call the

Synopsys-to-Xilinx constraints translator*/ /* utility **DC2NCF** to convert the ...
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Creating Timing Specifications

... analyze -f **vhdl** file1.vhd analyze -f **vhdl** file2.vhd . . . set_false_path...
write_script > "top.dc" sh **dc2ncf** "top.dc" exit. ...

[toolbox.xilinx.com/docsan/xilinx5/ data/docs/xsi/xsi0042_8.html](http://toolbox.xilinx.com/docsan/xilinx5/data/docs/xsi/xsi0042_8.html) - 40k - [Cached](#) - [Similar pages](#)

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Compiling a Synopsys CPLD Design

... To derive a logical design, based on your **VHDL**/HDL description, enter the following
Synopsys command: ... Enter the **dc2ncf** command at the Unix prompt as follows: ...

[www.xtra.xilinx.com/docsan/data/ alliance/syn/syn3_1.htm](http://www.xtra.xilinx.com/docsan/data/alliance/syn/syn3_1.htm) - 10k - [Cached](#) - [Similar pages](#)

Design Example

... Step 11 - Elaborate Your Design. To build the design based on your analyzed **VHDL**
file, entering the following Synopsys command: elaborate scan. ... **dc2ncf** scan.dc. ...

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2 SSK, A LTERA , X ILINX designSetup : syn ams | es2 | alt | xil A. M"ader ...

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[PDF]Synopsys Design Compiler Implementation Flow

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... EddieG Date: 6/29/98 SYNOPSYS Design Compiler SYNOPSYS Design Compiler **DC2NCF** Timing
Constraints Synopsys EDIF R Series Software ALLIANCE **VHDL** Verilog, EDIF ...

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... SYNOPSYS FGPA Compiler SYNOPSYS FGPA Compiler **DC2NCF** Timing Constraints
Synopsys

XNF Synthesis DesignWare Library R Series Software ALLIANCE **VHDL** Verilog, XNF ...

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rt.cs.tu-berlin.de/lehre/aes/flasher.script

... analyze -format **vhdl** TOP + ".vhd" /* == You ... Call the

Synopsys-to-Xilinx constraints translator*/ /* utility **DC2NCF** to convert ...

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... Einlesen der Designfiles, Überprüfen der Abhängigkeiten analyze -format vhd1 TOP
+ ".vhd" ... output TOP + ".db" write_script > TOP + ".dc" sh dc2ncf TOP + ".dc" ...

rt.cs.tu-berlin.de/lehre/aes/aes-flasher.pdf - [Similar pages](#)

Introduction to Synopsys to XACT M1 Toolset

... Run the **DC2NCF** program to translate any constraints you have placed on the design
in ... we will create a new design directory but copy the same **VHDL** source files ...

www.ee.qub.ac.uk/dsp/support/documentation/ synopsys_to_xact/intro_synopsys_xact.html - 16k - [Cached](#) -
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Standard Verilog-VHDL Interoperability Victor Berman Cadence Design

www.vhdl.org/vi/libutil/vhdl_verilog/interop.psA Versatile Design Validation Environment by Means of Software .. - Axel Jantsch (1994) (Correct)The hardware is simulated with the Synopsys **VHDL** simulator and the software is represented as C. A prototype board with two Xilinx XC4005 **FPGAs** and a local memory are connected to the systemwww.ele.kth.se/ESD/doc/ar94/axel/sims94.ps.gzAn EPLD Based Transient Recorder for Simulation of Video.. - Larsson University (Correct)Simulation of Video Signal Processing Devices in a **VHDL** Environment Close to System Level Conditions L.Hold/load 0 1 8 Reg 8 Fig. 3. Video Shifter **Fpga** Epld (fig. 4)In Replay Mode (play) Data Is Readtech-www.informatik.uni-hamburg.de/Personal/larsson/papers/epldtran_springer_lncs1142.ps.gzThe VHDL Standard - Meersman (1994) (Correct)/ Fax: 32(9)220.31.91 email: cme@e2s.be The **VHDL** Standard An overview of activities, organizationswww.vlsivie.tuwien.ac.at/mike/VHDLReport.ps

SpecCharts: A VHDL Front-End for Embedded Systems - Vahid (1995) (Correct) (8 citations)

. SpecCharts: A VHDL Front-End for Embedded Systems Frank Vahid,
www.cs.ucr.edu/~vahid/courses/269_f98/speccharts_tcad95.ps

The Virtual Wires Emulation System: A Gate-Efficient ASIC.. - Russell Tessier (1994) (Correct) (12 citations)
for Computer Science Cambridge, MA 02139 Abstract **FPGA**-based ASIC development systems have become Emulation System includes a number of tools to **translate** a design into a group of interconnected **FPGA** netlists. Each logic partition is subsequently **translated** into gates in the target **FPGA** technology and
ftp.cag.lcs.mit.edu/virtual_wires/fpga94.ps.Z

Sassy: A Language and Optimizing Compiler for Image.. - Hammes, Draper, Böhm (1999) (Correct) (1 citation)
in hardware description languages such as **VHDL**. Sassy was developed as part of the Cameron systems consist of field-programmable gate arrays (**FPGAs**) memories and interconnection hardware, and can
www.cs.colostate.edu/~draper/papers/hammes_icvs99.ps

Reconfigurable Hardware Approach To Build The Central Trigger.. - Cern Geneva (Correct)
option does not supported by the design tools for **VHDL** input feature. Generally **FPGA** devices contain the of the CTP critical components showed that **FPGA** devices could be considered as good candidates for
www1.cern.ch/RD27/note42.ps

A Design Methodology for Application Specific.. - Barriga.. (1998) (Correct)
be used to **translate** the XFL specification into a **VHDL** description capable of being implemented as a On-Line Verification Hardware Implementation Asic **Fpga** Xfl Xfsim Xflab Xfvhdl Design Stage Tool A synthesis tool, called xfvhdl, can be used to **translate** the XFL specification into a **VHDL** description
www.imse.cnm.es/online/1998/ICECS98.ABB.ps.gz

A Front-End VHDL Editor for Synthesis tools. - Bouguerba Benzakki (Correct)
A Front-End **VHDL** Editor for Synthesis tools. T. Bouguerba, J.
babar.inria.fr/pub/croap/General/VIUF_San-Diego.ps

A FPGA based Forth microprocessor - Leong Tsang (Correct)
board. The MSL16 design was synthesised from a **VHDL** description using the Synopsys Inc. **FPGA**
A **FPGA** based Forth microprocessor P. H. W. Leong, P. K.
www.cse.cuhk.edu.hk/~phwl/papers/fccm98_fcpsu.ps.gz

Formal Specification in VHDL for Hardware Verification - Reetz, Schneider, Kropf (Correct)
Formal Specification in **VHDL** for Hardware Verification Ralf Reetz Klaus
logics as in CV/CVC 1 timing diagrams **translated** into temporal logics [8] automata for
by the tool FLOWER, which has been implemented to **translate** verification bench descriptions into standard
goethe.ira.uka.de/~schneider/my_papers/ReSK98.ps.gz

An Assessment of the Suitability of FPGA-Based Systems for.. - Petersen, Hutchings (1995) (Correct)
(18 citations)
synthesizing simple high-level hardware language (**VHDL**) design statements (z la *b) These
An Assessment of the Suitability of **FPGA**-Based Systems for use in Digital Signal
splish.ee.byu.edu/docs/oxford_fpgadsp.ps.gz

Mesh Routing Topologies For FPGA Arrays - Scott Hauck (1994) (Correct) (3 citations)
February 1994. Mesh Routing Topologies For **FPGA** Arrays Scott Hauck, Gaetano Borriello, Carl
www.ece.nwu.edu/~hauck/publications/RoutingTop.ps

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